Abstract of the Disclosure

A method of monitoring the characteristics of a delay locked loop (DLL) in a memory device during a test mode is provided. The DLL generates an internal clock signal based on an external clock signal. The external and internal clock signals are normally synchronized. DLL constantly responds to variations in operating condition of the memory device to keep the external and internal clock synchronized. The method involves preventing the DLL from responding to a change in operating condition such as a change in the supply voltage of the memory device during a test mode.